AB32VG1 datasheet

BLUETRUM

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Introduction

1 Introduction

This document provides information on AB32VG1 microcontrollers, such as description, function overview, pin assignment, and definition, electrical characteristics and packaging.

2 Description

AB32VG1 devices are based on the 32-bit RISC-V core operating at up to 120MHz. AB32VG1 devices incorporate high-speed embedded memories with Flash memory of up to 1Mbyte, up to 192Kbytes of RAM.

- **Peripheral and Interfaces**
  - Three 32-bit timers;
  - Three multi-function 32-bit timers, support Capture and PWM mode;
  - WatchDog;
  - Three full-duplex UART;
  - Two SPI;
  - IR controller;
  - SD Card Host controller;
  - SPDIF receiver;
  - Audio interface IIS;
  - Full speed USB 2.0 HOST/DEVICE controller;
  - Sixteen Channels 10-bit SARADC;
  - Integrate IRTC;
  - Build in PMU, such as charger/buck/LDO;
- **Temperature**
  - Operating temperature: -40°C to +85°C;
  - Storage temperature: -65°C to +150°C;

3 Memories

3.1 Embedded Flash memory

The AB32VG1 devices embed up to 1Mbyte of Flash memory that can be used for storing programs and data.

3.2 Embedded SRAM

- SRAM0-SRAM3(0x10000-0x30000): 128Kbytes
- AECRAM, DECRAM, ENCRAM(0x50000-0x57a00): 30Kbytes
- ICRAM(0x60000-0x68000): 32Kbytes

4 Reset and clock controller

4.1 Clock management

The devices receives the following clock source inputs:

- **Internal oscillator**
  - 2MHz RC oscillator
- **External oscillator**
  - clock: 26MHz(generated form a crystal/ceramic resonator)

4.2 System reset sources

The product contains multiple reset sources,which include：

- POR reset
- MCLR reset
- WKP 10S reset
- LVD reset
- UART0 key match reset
- UART1 key match reset
- UART2 key match reset
- Wakeup software shut down reset
- VUSB insert reset
- WDT reset

The first three reset source will reset all chip except the part which in RTC, and the other reset sources will reset all chip except the part which in RTC or some register in CORE.

5 General purpose inputs/outputs(GPIOs)

Each of the GPIO pins can be configured by software as output (with pull-up or pull-down), as input (with pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption. In general, it has the following features:

1. Control GPIO input/output direction by using direction register
2. Internal pull-up/pull-down resistor by using pull-up/pull-down resistor control register
3. Select suitable output driving current capability

6 Audio decode

The audio decoding characteristics of the system are as follows:

1. Support MPEG1/2/2.5 decode
2. Support SBC decode

MPEG-1 decode：

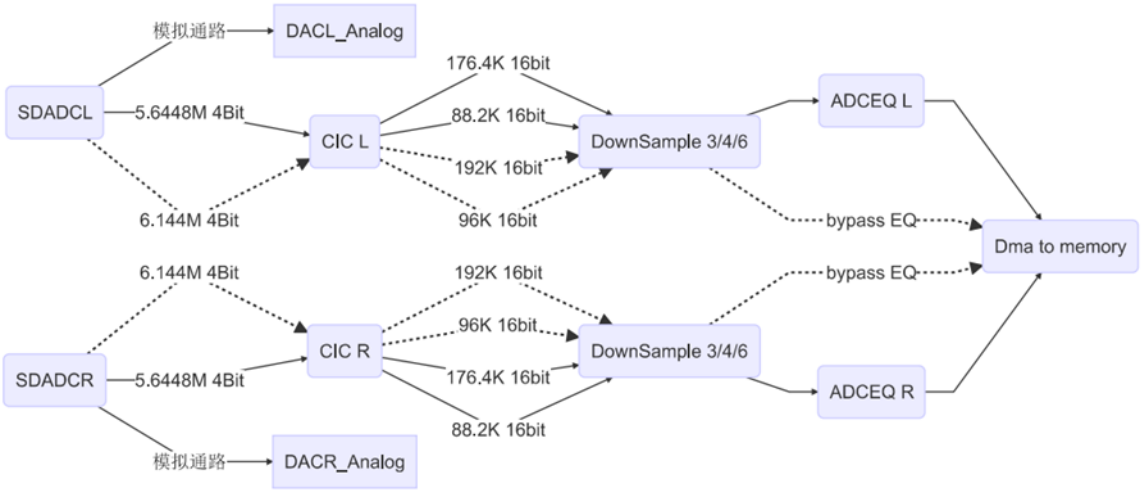
1. Support MPEG1/2/2.5 Layer III decode (Layer I,II coming later）
2. Support bit rate from 8K to 448K Kbit/s
3. Support sample frequency 8/11.025/12/16/22.5/24/32/44.1/48 KHz
4. Support working at system clock or diver n

SBC decode：

1. Support band 4/8
2. Support block 4/8/12/16

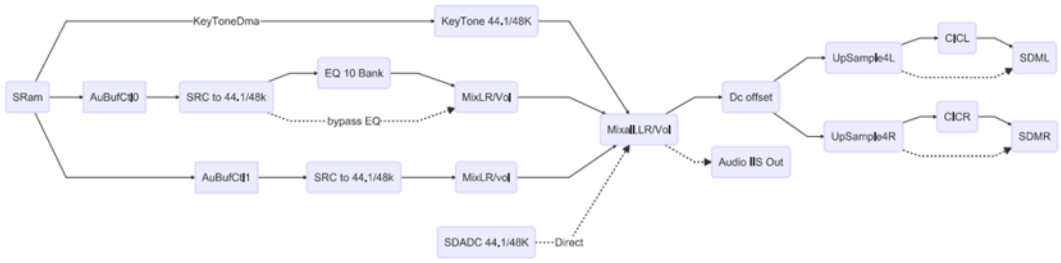
7 Analog to digital converter(ADC)

Audio codec with two channel 16bit ADC：



8 Digital to analog converter(DAC)

Audio codec with 16bit stereo DAC :



9 infrared-receiver(IR)

Infrared receiver is a device that can receive infrared signal and can independently complete the output from infrared signal compatible with TTL level signal. The infrared receiver(IR) features of the product are as follows:

1. Set IR RX bit select
2. Enable IR RX
3. Wait for pending or interrupt
4. Read IRRXDAT or detect RPTPND

10 Linear feedback shift register and cyclic redundant check(LFSR and CRC)

The Linear Feedback Shift Register (LFSR) is the linear function of the output, given the output of the previous state, used as the displacement register of the input.The xor operation is the most common single-bit linear function: the xor operation is performed on some bits of the register as input, followed by the whole shift of each bit in the register.

Cyclic Redundancy check (CRC) is a data transfer error check function that performs polynomial calculations on the data and attach the results to the frame. The receiving device performs a similar algorithm to ensure the correctness and integrity of the data transfer.If the CRC fails to pass, the system repeatedly copies the data to the hard disk, falling into an infinite loop, resulting in the replication process cannot be completed.

The features of the linear feedback shift register and cyclic redundancy check are as follows:

1. Support LFSR32: X32+X30+X26+X25
2. Support CRC16: X16+X12+X5+1

CRC16:

1. Select which data source
2. Write CRCDAT to calculate CRC16
3. Finish, can read CRCRES

LFSR32:

1. Select which data source
2. Write LFCRCCON bit8 to trigger LFSR
3. Finish, can read LFSRRES

11 Low power mode

The product supports two low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

11.1 sleep mode

Sleep mode will auto gate system clock, close memory access, close RC2M, but some asynchronous clock should be disable by software

Sleep mode wake up source as follow. After wakeup, software run continue or enter interrupt if enable:

1. BT wakeup
2. port external interrupt wakeup
3. RTC 1s or alarm wakeup
4. SPDIF online wakeup
5. IR receive data or repeat press wakeup

11.2 sniff mode

Sniff mode will auto gate system clock, close memory access, close RC2M, but some asynchronous clock should be disable by software. Sniff also change VDDIO/VDDCORE voltage by LPMCON

Sniff mode wake up source as follow. After wakeup, software run continues or enter interrupt if enable:

1. BT wakeup
2. Port external interrupt wakeup
3. RTC 1s or alarm wakeup
4. SPDIF online wakeup
5. IR receive data or repeat press wakeup

12 Pulse width modulation(PWM)

Four channel PWM for Breathing-lamp

13 Real time clock(RTC)

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary- coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

The system's features:

1. Support 32bit Independent power supply real time counter.
2. Support alarm interrupt and second interrupt.

14 Secure digital memory control(SD_CTL)

The system's SD card host controller can support SD/MMC card devices.

1. SD memory Card Spec (Ver2.0) / MMC Spec (Ver4.3) compatible.
2. CRC7 and CRC16 Generator.
3. Support Interrupt and DMA Data transfer mode.
4. Support 1-bit or 4-bit data bus width.
5. Support up to 50MHz in data transfer mode for SD.
6. Support up to 50MHz in data transfer mode for MMC.

15 Serial peripheral interface(SPI)

SPI can support different mode

1. general 3 wire mode, 1-bit clock in/out, 1-bit data output, 1-bit data input.
2. 2 wire mode, 1-bit clock in/out, 1-bit data output or input.
3. 2 data bus mode, 1-bit clock in/out, 2-bit data output or input.

SPI Normal 1bit-Mode Operation Flow:

1. Set 3-wire mode or 2-wire mode and select the pin map.
2. Select RXSEL for Transmit or receive.
3. Configure clock frequency .
4. Select one of the four timing mode.
5. Enable SPI module by setting SPIEN ‘1’.
6. Set SPIIE ‘1’ if needed.
7. Write data to SPIBUF to kick-start the process.
8. Wait for SPIPND to change to ‘1’, or wait for interrupt.
9. Read received data from SPIBUF if needed.
10. Go to Step 8 to start another process if needed or turn off SPI1by clearing SPIIE and SPIEN.

SPI Normal multi-bit-Mode Operation Flow:

1. Set data bus width(bus 2) and select the pin map.
2. Select RXSEL for Transmit or receive.
3. Configure clock frequency .
4. Select one of the four timing mode.
5. Enable SPI module by setting SPIEN ‘1’.
6. Set SPIIE ‘1’ if needed.
7. Write data to SPIBUF to kick-start the process.
8. If data bus width are 2 bit, write SPIBUF twice kick-start the transmission.
9. However, when receive data, only need write once to kick-start receive process.
10. Wait for SPIPND to change to ‘1’, or wait for interrupt.
11. Read received data from SPIBUF if needed.
12. Go to Step 8 to start another process if needed or turn off SPI by clearing SPIIE and SPIEN.

SPI DMA Mode Operation Flow:

1. Set IO in the correct direction and data width mode.
2. Select RXSEL for DMA direction.
3. Configure clock frequency .
4. Select one of the four timing modes.
5. Enable SPI module by setting SPIEN to ‘1’.

6. Set SPIIE ‘1’ if needed.
7. configure SPI1DMAADR.
8. Write data to SPI1_DMACNT to kick-start a DMA process.
9. Wait for SPIPND to change to ‘1’, or wait for interrupt.
10. Go to Step 8 to start another DMA process if needed or turn off SPI1 by clearing SPI1EN.

16 Timers

Timer0/1/2, only support 32bit timer function.

Timer3/4/5, can be configured to Timer-mode, Counter-mode, Capture-mode and PWM-mode.

17 Universal asynchronous receiver transmitter(UART)

It features:

UART is a serial port capable of asynchronous transmission.

The UART can function in full duplex mode.

18 Universal seria bus full speed(USB FS)

USB FS support 4 Endpoints (Endpoint 0, 1, 2, 3).Support Endpoint 0, Endpoint 1 and Endpoint 2 and Endpoint 3 supports both TX and RX transaction:

- EP0: RX/TX share 64 bytes
- EP1: RX is 64 bytes; TX is 64 bytes
- EP2: RX is 256 bytes; TX is 256 bytes
- EP3: RX is 1023 bytes; TX is 1023 bytes

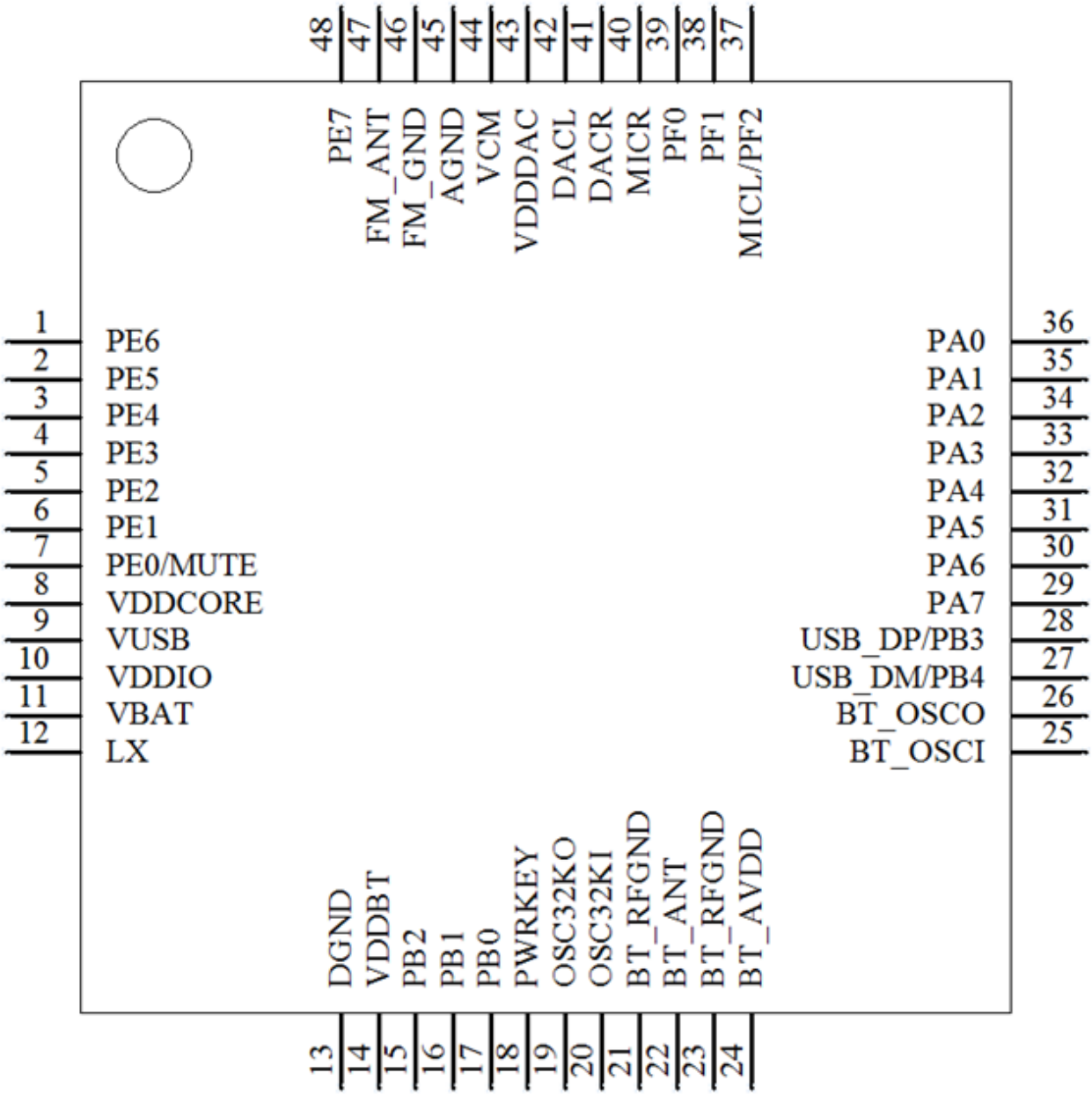
19 Watchdog timer(WDT)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

User guide:

1. configure WDT reset or interrupt
2. Select WDT time out
3. Clear WDT

20 Pinouts and pin description



21 Memory mapping

Table 1: memory mapping

	Memory	Size in Kbytes	Start address
RAM area	SRAM0	32	0X00010000
	SRAM1	32	0X00018000
	SRAM2	32	0X00020000
	SRAM3	32	0X00028000
	AECRAM	16	0X00050000
	DECRAM	12	0X00054000
	ENCRAM	2.5	0X00057000
	ICRAM	32	0X00060000
Code area	Flash memory	1024	0X10000000

22 Parameter conditions

23 Operating condition

23.1 PMU characteristics

23.2 I/O characteristics

23.3 DAC characteristics

23.4 ADC characteristics

23.5 BT characteristics

23.6 Current characteristics

23.7 Communications characteristics

24 Package information

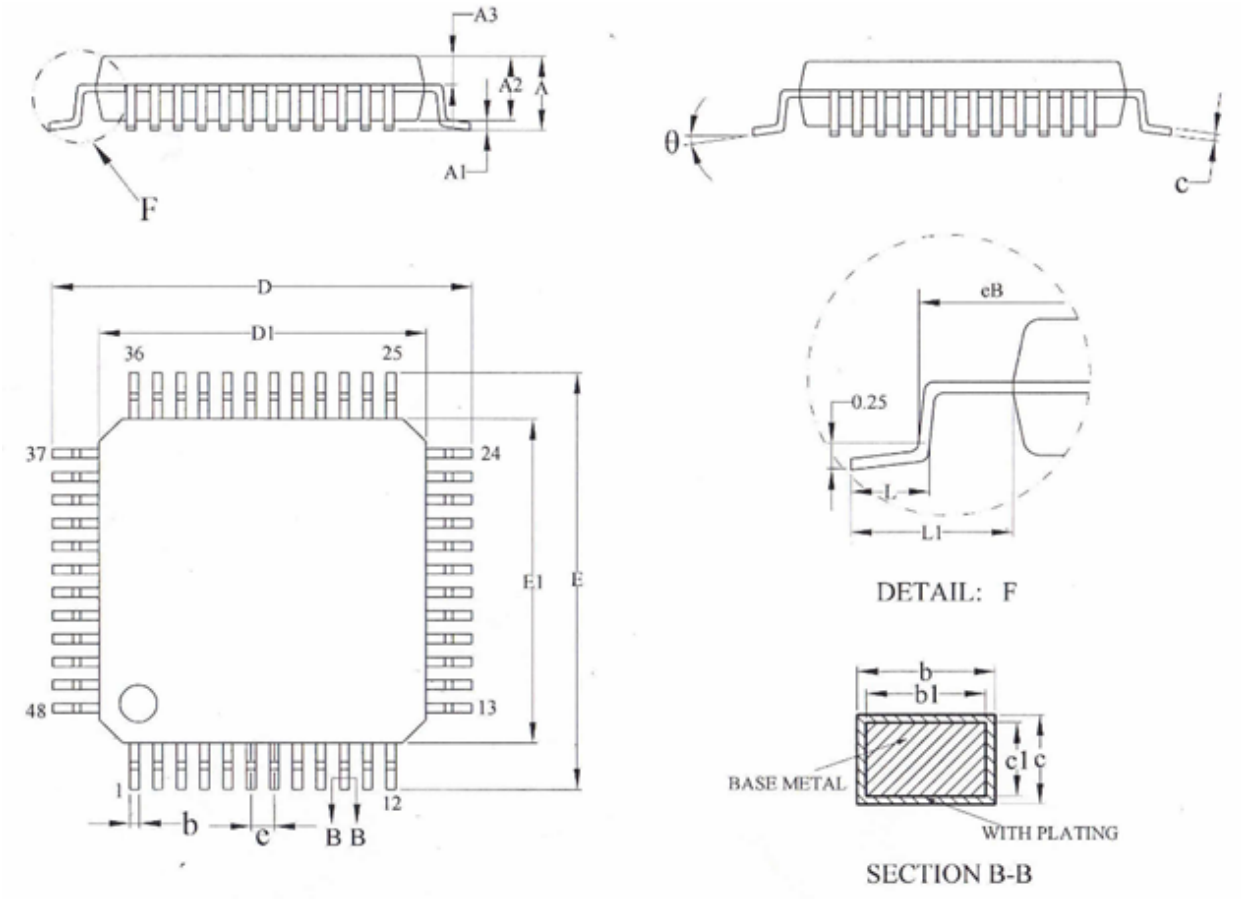


Table 2: Table Package Information

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	~	~	1.60
A1	0.05	~	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	~	0.26
b1	0.17	0x20	0.23
c	0.13	~	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	~	8.25
e	0.50BSC		
L	0.40	~	0.65
L1	1.00REF		
θ	0	~	7^o